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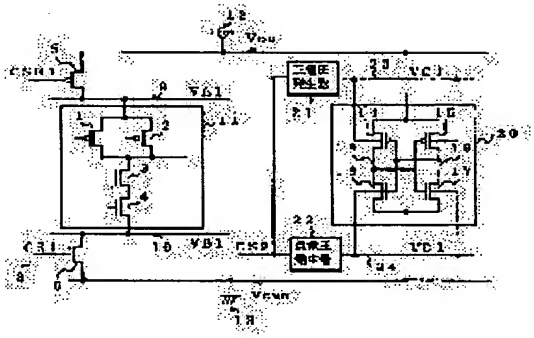
(54) SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the leakage current of a circuit which is not operated without destroying holding data of the sequential circuit and to reduce power consumption by providing a control means varying the threshold voltage of a fild effect transistor used in the sequential circuit.
SOLUTION: The sequential circuit 20 is constituted of (p) and (n) channel MOSFET 14-17 and the control means is constituted of a positive voltage generator 21, a negative voltage generator 22 and the back gate nodes 23 and 24 of the MOSFET 14-17. Nodes 18 and 19 form a pair of storage holding nodes. The positive voltage generator 21 and the negative voltage generator 22 set the potential VC1 and VD1 of the nodes 23 and 24 to be power voltage VDD and ground potential VGND when the sequential circuit 20 operates and set them to be higher than power voltage VDD and lower than ground potential VGND when the circuit does not operate. Thus, leak current is reduced and power consumption is reduced without destroying data of the storage holding nodes when the circuit does not operate.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor integrated circuit equipped with the switching means, the combinational circuit connected to this switching means, the sequential circuit containing the 1st field-effect transistor, and the control means which makes adjustable the threshold electrical potential difference of the 1st field-effect transistor of the above.
[Claim 2] It is the semiconductor integrated circuit according to claim 1 which the 1st field-effect transistor contained in a sequential circuit has the backgate, and is characterized by a control means making adjustable the threshold electrical potential difference of the 1st field-effect transistor of the above through this backgate.
[Claim 3] A control means is a semiconductor integrated circuit according to claim 2 characterized by including a forward voltage generator and a negative voltage generator.
[Claim 4] A semiconductor integrated circuit given [of claim 1 to the claims 3 which the 3rd field-effect transistor is contained in the switching means, and are characterized by the absolute value of the threshold electrical potential difference of the 3rd field-effect transistor of the above being higher than the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor of the above while the 2nd field-effect transistor is contained in the combinational circuit] in any 1 term.
[Claim 5] The 2nd field-effect transistor is contained in the combinational circuit, and 3rd at least two field-effect transistor is contained in the switching means. In the semiconductor integrated circuit by which the source of the transistor of another side is connected to ground potential while the source of the transistor of one of these is connected to supply voltage The absolute value of the threshold electrical potential difference of the 3rd field-effect transistor of the above spreads [the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor of the above] abbreviation etc. And a semiconductor integrated circuit given [of claim 1 to the claims 3 characterized by making potential between the gate sources into a reverse bias with the transistor by the side of supply voltage, and the transistor by the side of a ground when the 3rd field-effect transistor of the above is in an OFF state] in any 1 term.
[Claim 6] A combinational circuit is a semiconductor integrated circuit according to claim 1 characterized by consisting of two or more 1st circuit blocks, connecting the switching means according to the individual to each 1st circuit block, and connecting the control means which makes adjustable the threshold electrical potential difference of the 1st field-effect transistor by which a sequential circuit also consists of two or more 2nd circuit blocks, and is included in each 2nd circuit block according to an individual.
[Claim 7] A switching means is a semiconductor integrated circuit according to claim 6 characterized by having the reversal means connected with the 1st booster made to generate an electrical potential difference higher than supply voltage, the 1st pressure-lowering machine which generates an electrical potential difference lower than ground potential, and the 1st booster of the above, and the noninverting means connected with the pressure-lowering machine of the above 1st.
[Claim 8] A control means is a semiconductor integrated circuit according to claim 3 characterized by having the 2nd booster connected with a forward voltage generator, and the 2nd pressure-

lowering machine connected with a negative voltage generator, and the above-mentioned forward voltage generator and a negative voltage generator consisting of a multiplexer circuit.
[Claim 9] The semiconductor integrated circuit according to claim 8 characterized by the 2nd booster and the 2nd pressure-lowering machine which are contained in a control means differing from the 1st booster and the 1st pressure-lowering machine which are contained in a switching means.
[Claim 10] The semiconductor integrated circuit characterized by driving the control means controlled through the backgate of a field-effect transistor which has the backgate contained in a sequential circuit in the semiconductor integrated circuit equipped with the integrated circuit which has a logical circuit including a combinational circuit and a sequential circuit, and a booster and a pressure-lowering machine while driving the switching means of a combinational circuit using the booster and pressure-lowering machine of the above-mentioned integrated circuit.
[Claim 11] The semiconductor integrated circuit according to claim 10 characterized by the integrated circuit which has the above-mentioned booster and a pressure-lowering machine consisting of dynamic random access memory (DRAM).

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the low-power-ized semiconductor integrated circuit, in order to extend the battery life of a portable electronic device etc.
[0002]
[Description of the Prior Art] Low-power-izing a semiconductor integrated circuit (LSI) so that the long duration activity of the built-in cell can be further carried out with an advance and development of a pocket device in recent years is called for. Lowering operating voltage etc. is mentioned as effective technique for realizing low-power-ization. That is, since power consumption is given by the product of an electrical potential difference and a current, by reducing operating voltage, both an electrical potential difference and a current can be reduced and it is said that general has the effectiveness of square by this.
[0003] However, MOSFET which constitutes LSI has the property in which actuation deteriorates and speed becomes slow, when supply voltage is lowered. Even if this property reduces supply voltage, it originates in the ability of a threshold electrical potential difference not to be lowered carelessly. It is because the leakage current at the time of OFF of MOSFET increases and power consumption is made to increase on the contrary, if a threshold is reduced. In order to solve this technical problem, the following approaches were used conventionally.
[0004] Drawing 7 is a low-battery actuation circuit by the so-called MT-CMOS (Multi-threshold CMOS) of the former shown in JP,7-212218,A. In drawing, 1, 2, and 5 are p channel MOS FET, and 3, 4, and 6 are n channel MOS FET. While the absolute value of the threshold electrical potential difference of p channel MOS FET 1 and 2 is set up lower than the absolute value of the threshold of p channel MOS FET5, the absolute value of the threshold electrical potential difference of n channel MOS FET 3 and 4 is set up lower than the absolute value of the threshold of n channel MOS FET6 (a "threshold electrical potential difference" shall say the absolute value hereafter). And these MOSFETs 1-4 constitute the combinational circuit 11 of 2 input NAND gate. Moreover, it connects between supply voltage 12 and the imagination power-source line 9, and a control signal CSB 1 inputs p channel MOS FET5 into the gate, it connects between imagination earth wires 10 and grounds 13, and a control signal CS 1 inputs n channel MOS FET6 into the gate.
[0005] Next, actuation is explained. In operating the combinational circuit 11 of this 2 input NAND gate, while making a control signal CS 1 high-level, the control signal CSB 1 which is that reversal signal is made into a low level. Therefore, p channel MOS FET5 and n channel MOS FET6 will all be in the condition of ON, and can pull up the imagination power-source line 9 to the electrical-potential-difference VDD level of supply voltage 12, and, on the other hand, the imagination earth wire 10 is VGND of a ground 13. It is reduced to level. Consequently, this combinational circuit 11 will carry out the usual NAND actuation. Under the present circumstances, since the threshold electrical potential difference (absolute value) is set up low, also in case the electrical potential difference VDD of supply voltage 12 is a low battery, the high-speed actuation of MOSFETs 1-4 is attained.
[0006] When a combinational circuit 11 does not operate, a control signal CS 1 is made into a low level, and the control signal CSB 1 which is the reversal signal is made high-level. At this time, p

channel MOS FET5 and n channel MOS FET6 all become off, and the imagination power-source line 9 and the imagination earth wire 10 are separated from supply voltage 12 and a ground 13, respectively. Since a threshold electrical potential difference (absolute value) is higher than MOSFETs 1-4 and p channel MOS FET5 and n channel MOS FET6 are set up by each at this time, leakage current can be suppressed small.

[0007] Generally, the electrical potential difference between the gate sources of MOSFET increases the leakage current between source drains exponentially to gate voltage in the field below a threshold electrical potential difference. For this reason, when the combinational circuit 11 is not operating, leakage current can be substantially reduced by giving a difference to the threshold electrical potential difference of MOSFETs 1-4 and MOSFETs 5 and 6. In addition, although drawing 7 shows as an example the case where a combinational circuit 11 is 2 input NAND gate, the argument with this same in the circuit of any classes which constitute LSI, and magnitude is materialized.

[0008]

[Problem(s) to be Solved by the Invention] Since the semiconductor integrated circuit of the conventional low-battery actuation mold was constituted as mentioned above, in the case of the combinational circuit where it opts for an output with the combination of an input, it operated normally like 2 input NAND gate, but in the case of the sequential circuit which has the function which carries out storage maintenance of the former condition, the technical problem of causing malfunction occurred.

[0009] Drawing of the so-called latch circuit which the input and output of two inverters crossed mutually and was connected to drawing 8 as an example of this sequential circuit is shown. In drawing, p channel MOS FET, and 16 and 17 are n channel MOS FET, and 14 and 15 have a low threshold electrical potential difference (absolute value) for all. 5 is p channel MOS FET, 6 is n channel MOS FET, and both sides consist of what has a high threshold electrical potential difference (absolute value). A sequential circuit 20 is constituted by these MOSFETs 14-17, nodes 18 and 19 form the storage maintenance node of a couple, and when one of these is high-level, the value which another side was set to a low level and inputted can be held.

[0010] Next, actuation is explained. When a sequential circuit 20 operates where CSB1 is set to a low level while CS1 is high-level, the value of the written-in data is held normally, and since both the threshold electrical potential differences of p channel MOS FET 14 and 15 and n channel MOS FET 16 and 17 are low, moreover, writing and read-out to nodes 18 and 19 can be performed at a high speed.

[0011] If CS1 is moreover set to CSB1 being high-level with a low level and leakage current decreases, while not operating, since the direction of the leakage current at the time of the OFF in MOSFETs 14-17 will become larger than the leakage current at the time of OFF of MOSFETs 5 and 6, it becomes impossible however, to hold the data of nodes 18 and 19. It is because the node 18 high-level [a node 18 is high-level, and] by the favor of leakage current which flows p channel MOS FET15 and n channel MOS FET16 although p channel MOS FET15 and n channel MOS FET16 will become off among MOSFETs 14-17 and other two will become ON, supposing a node 19 is a low level falls, for example and the node 19 of a low level goes up. This will continue until the level of nodes 18 and 19 becomes equal, and the data currently held as a result will be lost. Thus, in the semiconductor integrated circuit of the conventional low-battery actuation mold, the technical problem that the data of a sequential circuit will disappear occurred.

[0012] It aims at obtaining the semiconductor integrated circuit which can attain low-power-ization by reduction of the leakage current of the circuit which is not operating, without having been made in order that this invention might solve the above technical problems, and destroying the maintenance data of a sequential circuit.

[0013]

[Means for Solving the Problem] The semiconductor integrated circuit concerning invention according to claim 1 is equipped with a switching means, the combinational circuit connected to this switching means, the sequential circuit containing the 1st field-effect transistor, and the control means which makes adjustable the threshold electrical potential difference of the 1st field-effect transistor.

[0014] The 1st field-effect transistor in which the semiconductor integrated circuit concerning invention according to claim 2 is contained in a sequential circuit has the backgate, and a control means makes adjustable the threshold electrical potential difference of said 1st field-effect transistor through this backgate.
[0015] In the semiconductor integrated circuit concerning invention according to claim 3, a control means contains a forward voltage generator and a negative voltage generator.
[0016] The 3rd field-effect transistor is contained in the switching means, and the semiconductor integrated circuit concerning invention according to claim 4 has the absolute value of the threshold electrical potential difference of the 3rd field-effect transistor higher than the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor while the 2nd field-effect transistor is contained in the combinational circuit.
[0017] The semiconductor integrated circuit concerning invention according to claim 5 The 2nd field-effect transistor is contained in the combinational circuit, and 3rd at least two field-effect transistor is contained in the switching means. In the semiconductor integrated circuit by which the source of the transistor of another side is connected to ground potential while the source of the transistor of one of these is connected to supply voltage The absolute value of the threshold electrical potential difference of the 3rd field-effect transistor spreads [the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor] abbreviation etc. And when the 3rd field-effect transistor of the above is in an OFF state, let potential between the gate sources be a reverse bias with the transistor by the side of supply voltage, and the transistor by the side of a ground.
[0018] It consists of the 1st circuit block of plurality [semiconductor integrated circuit / concerning invention according to claim 6 / combinational circuit], and the control means to which a switching means makes adjustable the threshold electrical potential difference of the 1st field-effect transistor which it connects according to the individual, and a sequential circuit also consists of two or more 2nd circuit blocks, and is contained in each 2nd circuit block is connected according to the individual to each 1st circuit block.
[0019] The semiconductor integrated circuit concerning invention according to claim 7 is equipped with the reversal means connected with the 1st booster made to generate an electrical potential difference higher than supply voltage, the 1st pressure-lowering machine which generates an electrical potential difference lower than ground potential, and the 1st booster, and the noninverting means connected with the 1st pressure-lowering machine by the switching means.
[0020] As for the semiconductor integrated circuit concerning invention according to claim 8, the control means is equipped with the 2nd booster connected with a forward voltage generator, and the 2nd pressure-lowering machine connected with a negative voltage generator, and a forward voltage generator and a negative voltage generator consist of a multiplexer circuit.
[0021] The semiconductor integrated circuit concerning invention according to claim 9 differs from the 1st booster and the 1st pressure-lowering machine with which the 2nd booster and the 2nd pressure-lowering machine which are contained in a control means are contained in a switching means.
[0022] In the semiconductor integrated circuit equipped with the integrated circuit which has a logical circuit including a combinational circuit and a sequential circuit, and a booster and a pressure-lowering machine, the semiconductor integrated circuit concerning invention according to claim 10 drives the control means controlled through the backgate of a field-effect transistor which has the backgate contained in a sequential circuit while driving the switching means of a combinational circuit using the booster and pressure-lowering machine of an integrated circuit.
[0023] The integrated circuit with which the semiconductor integrated circuit concerning invention according to claim 11 has a booster and a pressure-lowering machine consists of dynamic random access memory (DRAM).
[0024]
[Embodiment of the Invention] Hereafter, one gestalt of implementation of this invention is explained.
Gestalt 1. drawing 1 of operation is drawing showing the semiconductor integrated circuit of the low-battery actuation mold by the gestalt 1 of implementation of this invention, and, for p channel

MOS FET and 5, p channel MOS FET, and 3 and 4 is [1 and 2 / n channel MOS FET 23 and 24 of n channel MOS FET and 6] the nodes for backgates in drawing. Here, while the absolute value of the threshold electrical potential difference of p channel MOS FET 1 and 2 is set up lower than the absolute value of the threshold electrical potential difference of p channel MOS FET5, the absolute value of the threshold electrical potential difference of n channel MOS FET 3 and 4 is set up lower than the absolute value of the threshold electrical potential difference of n channel MOS FET6 (a "threshold electrical potential difference" shall say the absolute value hereafter). And these MOSFETs 1-4 constitute a combinational circuit 11 like 2 input NAND gate, and MOSFETs 5 and 6 constitute a switching means. In this case, it connects between supply voltage 12 and the imagination power-source line 9, and a control signal CSB 1 inputs p channel MOS FET5 into that gate. Moreover, it connects between imagination earth wires 10 and grounds 13, and a control signal CS 1 inputs n channel MOS FET6 into the gate.

[0025] On the other hand, as for 14 and 15, p channel MOS FET, and 16 and 17 are n channel MOS FET, and these constitute the sequential circuit 20. Moreover, the forward voltage generator 21, the negative voltage generator 22, and the nodes 23 and 24 for backgates of MOSFETs 14-17 constitute the control means. These MOSFETs 14-17 consist of what has the low absolute value of a threshold electrical potential difference, and nodes 18 and 19 form the storage maintenance node of a couple. In this case, it has the composition of having connected the backgate potential VC 1 of p channel MOS FET 14 and 15 to the output of the forward voltage generator 21, and having connected the backgate potential VD1 of n channel MOS FET 16 and 17 to the output of the negative voltage generator 22.

[0026] Next, actuation is explained. In operating a combinational circuit 11, while making a control signal CS 1 high-level, the control signal CSB 1 which is the reversal signal is made into a low level. Thereby, p channel MOS FET5 and n channel MOS FET6 will all be in the condition of ON, and can pull up the imagination power-source line 9 to the potential VDD level of supply voltage 12, and, on the other hand, the imagination earth wire 10 is VGND of a ground 13. It is reduced to level. Consequently, the combinational circuit 11 of such a 2 input NAND gate will carry out the usual NAND actuation. Under the present circumstances, since the threshold electrical potential difference (absolute value) of MOSFETs 1-4 is set up low, also in case the electrical potential difference of supply voltage 12 is a low battery, the high-speed actuation of it is attained with a low power.

[0027] In not operating a combinational circuit 11, a control signal CS 1 is made into a low level, and it makes high-level the control signal CSB 1 which is the reversal signal. At this time, p channel MOS FET5 and n channel MOS FET6 all become off, and the imagination power-source line 9 and the imagination earth wire 10 are separated from supply voltage 12 and a ground 13, respectively. Here, since p channel MOS FET5 and n channel MOS FET6 are set up more highly than MOSFETs 1-4 by each in the threshold electrical potential difference (absolute value), they can suppress leakage current small.

[0028] On the other hand, while the control signal CS 2 inputted into a control means becomes high-level at the time of actuation and the backgate potential VC 1 of p channel MOS FET 14 and 15 serves as supply voltage VDD level with the forward voltage generator 21 about a sequential circuit 20, the backgate potential VD1 of n channel MOS FET 16 and 17 is the ground potential VGND by the negative voltage generator 22. It is set to level. Therefore, a sequential circuit 20 can perform the usual storage maintenance actuation at this time. In this case, since p channel MOS FET 14 and 15 and n channel MOS FET 16 and 17 of a sequential circuit 20 have the all low absolute value of a threshold electrical potential difference and are constituted, they can perform writing and read-out of the data to nodes 18 and 19 at a high speed. Moreover, when a sequential circuit 20 does not operate, CS2 is set to a low level, the output VC 1 of the forward voltage generator 21 becomes higher than supply voltage VDD, and the output VD1 of the negative voltage generator 22 is the ground potential VGND. It becomes a low value. Consequently, since the threshold electrical potential difference becomes high since the backgate potential VC 1 of p channel MOS FET 14 and 15 becomes higher than supply voltage 12, and the backgate potential VD1 concerning the backgate of n channel MOS FET 16 and 17 becomes [potential] lower than supply voltage 12, a threshold electrical potential difference becomes high too. For this reason, the

leakage current which flows from the supply voltage 12 of a sequential circuit 20 to a ground 13 can be reduced.
[0029] As mentioned above, according to the gestalt 1 of this operation, it is effective in decreasing power consumption, without reducing leakage current and destroying the data of a storage maintenance node by changing the backgate potential of low threshold MOSFET and raising that threshold electrical potential difference, when not operating a sequential circuit 20. Furthermore, since the threshold of MOSFET currently used for the combinational circuit 11 and the sequential circuit 20 is low, there is effectiveness that a high speed and a low power can perform writing and read-out, also at the time of actuation. In addition, although the gestalt 1 of this operation explained control signals CS1 and CS2 as another signal, even if both are the same signals, same actuation can be realized, and the same effectiveness is done so.
[0030] Gestalt 2. drawing 2 of operation is drawing showing the semiconductor integrated circuit of the low-battery actuation mold by the gestalt 2 of implementation of this invention, and in drawing, since the configuration and actuation of a sequential circuit 20 are the same as that of the gestalt 1 of operation, they give the same sign to the same part, and omit duplication explanation. In the gestalt 2 of this operation, the threshold electrical potential difference of MOSFETs 5 and 6 for leakage current reduction in case a combinational circuit 11 does not operate is set as the same low threshold electrical potential difference as other MOSFETs 1-4.
[0031] Next, actuation is explained. When not operating a combinational circuit 11 with the gestalt 2 of this operation, it is Ground VGND about a control signal CS 1. While considering as low potential, reduction of leakage current is aimed at by making CSB1 into potential higher than supply voltage VDD. Otherwise, it is because the threshold of MOSFET which constitutes a switching means is comparable as what constitutes a combinational circuit, so leak of a current occurs between a power source and a ground and the consumed electric power of the whole circuit increases the way things stand. Therefore, if constituted as mentioned above, the same effectiveness as the gestalt 1 of operation is not only acquired, but a threshold can make all low including MOSFETs 5 and 6 used for a switching means, without using MOSFET which has two or more kinds of threshold electrical potential differences. Therefore, the number of masks can be decreased at the time of a fabrication of semiconductor integrated circuit equipment, and since a fabrication routing counter can be reduced, there is effectiveness of manufacturing-cost reduction.

[0032] Gestalt 3. drawing 3 of operation is the block diagram showing the case where the circuit block which consists of the combinational circuit and sequential circuit of each plurality by the gestalt 3 of implementation of this invention is applied to a large-scale integrated circuit (LSI), and is set to drawing. 111-11m It is the block of a combinational circuit and each is a control signal CSB 11 - CSB1m. 51-5m of p channel MOS FET to input A control signal CS 11 - CS1m 61-6m of n channel MOS FET to input It provides. On the other hand, it is 201-20n. It is the block of a sequential circuit and each is CS21 - CS2n. 211-21n of forward voltage generators to input, 221-22n of negative voltage generators 231-23n (control means) of nodes for backgates, and 241-24n It provides. Since other configurations are the same as the gestalt 2 of operation shown in said drawing 2 , they give the same sign to the same part, and omit duplication explanation.
[0033] 111-11m of blocks of a combinational circuit It sets and is 51-5m of p channel MOS FET. It has the low threshold and they are a control signal CSB 11 - CSB1m. The same work as p channel MOS FET5 of the gestalt 2 of operation is carried out, and it is 61-6m of n channel MOS FET. They are a control signal CS 11 - CS1m at a low threshold. The same work as n channel MOS FET of the gestalt 2 of operation is carried out. 211-21n of moreover, forward voltage generators The same work as the forward voltage generator 21 of the gestalt 1 of operation is carried out, and each is a control signal CS 21 - CS2n. 201-20n of sequential circuits 231-23n of nodes for backgates of p channel MOS FET It controls. On the other hand, it is 201-20n of blocks of a sequential circuit. It sets and is 221-22n of negative voltage generators. The same work as the negative voltage generator 22 of the gestalt 1 of operation is carried out, and each is 201-20n of sequential circuits by the control signal CS 21 - CS2n. 231-23n of nodes for backgates of n channel MOS FET It controls. In addition, a control signal CSB 11 - CSB1m, CS11 - CS1m, and a control signal CS 21 - CS2n Each shall operate independently.

[0034] Next, actuation is explained. 111-11m of blocks of a combinational circuit It receives and they are a control signal CSB 11 - CSB1m, and CS11 - CS1m. By making it input independently, respectively 111-11m of blocks of a combinational circuit It operates independently, respectively and, on the other hand, is 201-20n of blocks of a sequential circuit. It receives and they are a control signal CS 21 - CS2n similarly. By inputting independently, respectively 201-20n of blocks of a sequential circuit It operates independently, respectively.
[0035] As mentioned above, since actuation of the sequential circuit when not operating is independently controllable for every block of a sequential circuit according to the gestalt 3 of this operation Leakage current can be controlled and reduced according to an individual so that the data currently held by each storage maintenance node may not be destroyed, and since MOSFET which moreover has two or more kinds of thresholds is not used, it can contribute to reduction of the number of production processes by reduction of the number of masks etc. Therefore, the effectiveness which controls the power consumption by the cutback of a manufacturing cost and reduction of the leakage current of the part into which the semiconductor integrated circuit produced commercially is not operating in the time of standby etc. is acquired. In addition, although explained on the basis of the semiconductor integrated circuit of drawing 2 R> 2, it may be based on the semiconductor integrated circuit of drawing 1 here.
[0036] Gestalt 4. drawing 4 of operation is drawing showing the circuitry of the semiconductor integrated circuit by the gestalt 4 of implementation of this invention, and is a control signal CSB 11 - CSB1m. And CS11 - CS1m The case where it is made to generate using a booster and a pressure-lowering machine is shown. The booster made to generate an electrical potential difference with 48 [higher than supply voltage] in drawing (the 1st booster), The pressure-lowering machine made to generate an electrical potential difference with 49 [lower than ground potential] (1st pressure-lowering machine), 501-50m Control signal BE1 -BEm The buffer circuit which has an inverting function, 511-51m Control signal BE1 -BEm It is the buffer circuit which has a noninverting function, and is 501-50m of buffer circuits. 511-51m of non-buffer circuits A reversal means and a noninverting means are constituted, respectively. VH VL The output and ground potential VGND of the booster 48 which has potential respectively higher than supply voltage VDD It is the output of the pressure-lowering machine 49 which has low potential. 501-50m of moreover, reversal buffer circuits They are node ND11 and a node ND 21, —, node ND1m and node ND2m about a power source and a ground, respectively. It connects and is 511-51m of noninberting buffer circuits. They are node ND31 and a node ND 41, —, node ND3m and node ND4m about a power source and a ground, respectively. It connects. Control signal BE1 -BEm CSB11 and CS11 which is the control signal inputted into a combinational circuit, —, CSB1m and CS1m It is a signal for controlling. Since other configurations are the same as the gestalt 3 of operation shown in said drawing 3 , they give the same sign to the same part, and omit duplication explanation.
[0037] Next, actuation is explained. One [111] of m combinational circuit blocks shown in drawing 3 If it takes for an example, when operating, it is a control signal BE1. It becomes high-level. At this time, it is a buffer circuit 501. And 511 It sets and is CSB11. And CS11 It is Ground VGND, respectively. And it is set to the level of supply voltage VDD, and actuation explained with the gestalt 3 of operation is performed. When not operating, it is a control signal BE1. It is set to a low level and is CSB11 at this time. Reversal buffer circuit 501 Node ND 11 which leads, is reversed and has potential higher than supply voltage VDD Potential VH It becomes and is CS11. Noninberting buffer circuit 511 Node ND 41 which leads, and noninverting is carried out and has potential lower than a ground Potential VL It becomes. Thereby, it is the combinational circuit block 111 like what was explained with the gestalt 3 of operation. Leakage current can be reduced. the same -- 50m of buffer circuits, and 51m etc. -- also being related -- control signal BEm Above-mentioned actuation is carried out.
[0038] As mentioned above, since the leakage current when not operating the combinational circuit can be further reduced only by adding simple circuits, such as a booster and a pressure-lowering machine, to a reversal buffer circuit and a noninberting buffer circuit according to the gestalt 4 of this operation, it is effective in the ability to reduce further the power consumption by the leakage current of the part which is not operating with a semiconductor integrated circuit. In addition, the

gestalt 4 of this operation may prepare above-mentioned pressure up and pressure-lowering circuit in the same chip as the circuit which consists of a combinational circuit and a sequential circuit shown in the gestalt 3 of operation, and has the effectiveness which can reduce the size of the chip which loaded the semiconductor integrated circuit by this.
[0039] It is drawing showing the circuitry of the semiconductor integrated circuit by the gestalt 5 of implementation of this invention, it sets to drawing, and gestalt 5. drawing 5 of operation is 581-58n. It is 211-21n of forward voltage generators, respectively. A multiplexer circuit (MUX) and 591-59n to constitute It is 221-22n of negative voltage generators, respectively. It is the multiplexer circuit (MUX) to constitute. Since other configurations are the same as the gestalt 4 of operation, they give the same sign to the same part, and omit duplication explanation.
[0040] Next, actuation is explained. For example, sequential circuit 201 in drawing 3 When operating, a control signal CS 21 becomes high-level, and it is the multiplexer circuit 581. It sets, supply voltage VDD is chosen and it is the node 231 for backgates. It is outputted and is the multiplexer circuit 591. It sets and is the ground potential VGND. Node 241 for backgates It is outputted. When not operating, it is a control signal CS 21. It is set to a low level and is the multiplexer circuit 581. It sets and is the potential VH higher than supply voltage. It is chosen and is the node 231 for backgates. It is outputted and is the multiplexer circuit 591. It sets and is the potential VL lower than ground potential. It is chosen and is the node 241 for backgates. It is outputted. Thereby, the same actuation as the gestalt 3 of operation is realized.
[0041] As mentioned above, since according to the gestalt 5 of this operation it constituted so that a simple and cheap multiplexer circuit might be applied to forward and a negative voltage generator, even while not operating the sequential circuit, leakage current can be reduced, and the maintenance data of a sequential circuit are not destroyed. Therefore, there is effectiveness which reduces the power consumption of the part which is not operating with a semiconductor integrated circuit with a low manufacturing cost. In addition, although the gestalt 5 of this operation explained the booster (the 2nd booster) 48 and the pressure-lowering machine (2nd pressure-lowering machine) 49 as the same thing as the thing of the gestalt 4 of operation, if it enables it to set up output voltage for these uniquely as another thing, reduction of finer leakage current is realizable. Furthermore, the circuit which consists of forward and the negative voltage generator shown in the gestalt 5 of this operation may be prepared in the same chip as the circuit which consists of a combinational circuit and a sequential circuit shown in the gestalt 3 of operation, and there is effectiveness which can reduce the size of the chip which loaded the semiconductor integrated circuit by this.
[0042] Gestalt 6. drawing 6 of operation is drawing showing the circuitry of the semiconductor integrated circuit by the gestalt 6 of implementation of this invention, 62 is the high accumulation [need / the storage information represented by a flash memory and dynamic random access memory (DRAM) / to be refreshed] MOSRAM in drawing, and 63 is a logical circuit and is the so-called hybrid mold semiconductor integrated circuit of the type which the memory section and the logic section loaded together. A logical circuit is taken as the same configuration as the logical circuit which consists of a combinational circuit and a sequential circuit in the gestalt 3 of operation. Since it is necessary to operate a circuit good like refresh actuation in the high accumulation MOSRAM, the booster 48 and the pressure-lowering machine 49 are formed in the interior of usual, and they are these outputs VH and VL. If it applies to a logical circuit 63, it can be made to operate like the gestalt 3 of operation.
[0043] As mentioned above, according to the gestalt 6 of this operation, since the booster and pressure-lowering machine which are arranged inside DRAM can be used effectively, the occupancy area of an additional circuit can be reduced, therefore the increment in the number of components of hardware can be controlled. Consequently, since it not only contributes to the cutback of power consumption based on reducing the leakage current of the part which is not operating with a semiconductor integrated circuit, but the chip size of the done semiconductor integrated circuit equipment can be made small, it is effective in reducing a manufacturing cost.
[0044]
[Effect of the Invention] As mentioned above, since according to invention according to claim 1 the 1st field-effect transistor currently used for the sequential circuit was constituted so that a

control means could make the threshold electrical potential difference adjustable A low power can perform writing and read-out of the data to the storage maintenance node which made low the threshold electrical potential difference of the 1st field-effect transistor, and was formed in this sequential circuit when a sequential circuit operated at a high speed. In addition, when a sequential circuit does not operate, by raising the threshold electrical potential difference of the 1st field-effect transistor, leakage current can be decreased and there is effectiveness which does not break and disappear the data currently held by this at the storage maintenance node. Moreover, since the switching means was constituted so that it could separate from other circuit parts when a combinational circuit did not operate, it is effective in the ability to reduce the leakage current of a combinational circuit.

[0045] Since according to invention according to claim 2 the 1st field-effect transistor which constitutes a sequential circuit was constituted so that it might have a backgate, when not operating a sequential circuit, and a control means controls the potential through a backgate, the threshold of the 1st field-effect transistor can be raised, leakage current can be decreased, and it is effective in bringing about prevention and low-power-izing of destruction and disappearance in the data currently held by this at the storage maintenance node.

[0046] Since according to invention according to claim 3 it constituted so that the control means linked to a sequential circuit might contain a forward voltage generator and a negative voltage generator, the control signal inputted into the forward voltage generator and the negative voltage generator linked to a backgate can make adjustable the threshold of the 1st field-effect transistor of the p channel section which constitutes a sequential circuit from high level or a low level, and the n channel section. therefore, since a transistor is operated with a low threshold when operating a sequential circuit, when there is little the power consumption, it moreover ends with rapid access and it does not operate on the other hand While making it become higher than supply voltage, the threshold of the transistor of the p channel section Since the threshold of the transistor of the n channel section can be made lower than ground potential, the leakage current which flows from the power source of a sequential circuit to a ground can be reduced, and there is effectiveness which does not disappear the maintenance data which are in a storage maintenance node by this. Furthermore, if a sequential circuit is constituted using the transistor which has the above-mentioned backgate, since a threshold is able to constitute this from a small transistor, reduction of a manufacturing cost is brought about by reduction of the routing counter accompanying reduction of the number of masks, and since the chip size of the semiconductor integrated circuit equipment of completion can moreover be decreased, it is effective in improving the product yield.

[0047] According to invention according to claim 4, since it is constituted so that smaller than the threshold electrical potential difference of the 3rd field-effect transistor used for the switching means, the threshold electrical potential difference of the 2nd field-effect transistor used for the combinational circuit is effective in the ability of a low power to perform logic actuation at a high speed only by stopping the level of the control signal sent to the gate of a combinational circuit.

[0048] According to invention according to claim 5, the threshold electrical potential difference of the 2nd field-effect transistor used for the combinational circuit Spread a threshold electrical potential difference of the 3rd field-effect transistor, abbreviation, etc. which are used for the switching means. Since the 3rd field-effect transistor was constituted so that the electrical potential difference between the gate sources might be made into a reverse bias with the transistor by the side of supply voltage, and the transistor by the side of a ground when it was in an OFF state A transistor with a small threshold is applicable just like that by which the transistor used for the above-mentioned switching means is also used for a combinational circuit. Therefore, since the transistor which has the threshold of varieties in one semiconductor integrated circuit is not made intermingled, the number of masks is decreased, a fabrication process is simplified, and it is effective in reducing a manufacturing cost.

[0049] According to invention according to claim 6, a combinational circuit consists of two or more circuit blocks. The switching means is connected according to the individual to each circuit block. Since it constituted as the control means which makes adjustable the threshold electrical potential difference of the 1st field-effect transistor by which a sequential circuit also consists of two or more circuit blocks, and is included in each circuit block was connected according to the individual

There is effectiveness which can control leakage current finely and can be prevented from disappearing the storage maintenance data of a sequential circuit taking into consideration terms and conditions, such as power consumption, an access rate, etc. of a semiconductor integrated circuit.

[0050] Since according to invention according to claim 7 the 1st booster and pressure-lowering machine can control independently the potential built between the gate sources of the 3rd field-effect transistor which a switching means has by the power-source and ground side, respectively in case a control signal goes via a reversal means and a noninverting means, it can consider as a reverse bias mutually. Since the leakage current of a combinational circuit can be reduced by addition of a simple circuit by this, there is effectiveness which contributes to low-power-ization.

[0051] According to invention according to claim 8, the control means linked to a sequential circuit is equipped with the 2nd pressure-lowering machine connected with the 2nd booster connected with a forward voltage generator, and a negative voltage generator. Since the forward voltage generator and the negative voltage generator were constituted so that it might consist of a simple multiplexer circuit, when a sequential circuit does not operate, the control signal which went via the multiplexer circuit can be set up so that the leakage current of a sequential circuit may be reduced more by the booster and pressure-lowering machine side through a backgate. Therefore, it is effective in the ability to reduce the power consumption of a circuit further only by adding a simple and cheap circuit, without disappearing storage maintenance data.

[0052] Since it was made for the booster and pressure-lowering machine contained in a control means to constitute independently of what is contained in a switching means according to invention according to claim 9, output voltage can be set up according to an individual, reduction of finer leakage current can be realized, and there is effectiveness which contributes to power-saving of the done whole semiconductor integrated circuit equipment.

[0053] Since according to invention according to claim 10 it constituted as the logical circuit including the circuit containing a booster and a pressure-lowering machine, and a combinational circuit and a sequential circuit joined together, if the booster and pressure-lowering machine of an integrated circuit are diverted to this logical circuit, since setting out of an additional circuit is omissible,-izing of the chip size of the whole semiconductor integrated circuit equipment can be carried out [****]. And there is effectiveness which can contribute also to reduction of the fabrication cost per one-sheet wafer by reduction in a chip size.

[0054] Since according to invention according to claim 11 it constituted so that the integrated circuit which has a booster and a pressure-lowering machine might consist of dynamic random access memory (DRAM), the hybrid circuit of a logical circuit and DRAM can be created, and since DRAM possesses a booster and a pressure-lowering machine for refresh actuation etc., it can usually be designed so that these may be used for logical circuit actuation. Therefore, there is effectiveness which cannot cause buildup of the number of components and can contribute to cutback-ization of the occupancy area of the whole hybrid circuit.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention relates to the low-power-ized semiconductor integrated circuit, in order to extend the battery life of a portable electronic device etc.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Low-power-izing a semiconductor integrated circuit (LSI) so that the long duration activity of the built-in cell can be further carried out with an advance and development of a pocket device in recent years is called for. Lowering operating voltage etc. is mentioned as effective technique for realizing low-power-ization. That is, since power consumption is given by the product of an electrical potential difference and a current, by reducing operating voltage, both an electrical potential difference and a current can be reduced and it is said that general has the effectiveness of square by this.

[0003] However, MOSFET which constitutes LSI has the property in which actuation deteriorates and speed becomes slow, when supply voltage is lowered. Even if this property reduces supply voltage, it originates in the ability of a threshold electrical potential difference not to be lowered carelessly. It is because the leakage current at the time of OFF of MOSFET increases and power consumption is made to increase on the contrary, if a threshold is reduced. In order to solve this technical problem, the following approaches were used conventionally.

[0004] Drawing 7 is a low-battery actuation circuit by the so-called MT-CMOS (Multi-threshold CMOS) of the former shown in JP,7-212218,A. In drawing, 1, 2, and 5 are p channel MOS FET, and 3, 4, and 6 are n channel MOS FET. While the absolute value of the threshold electrical potential difference of p channel MOS FET 1 and 2 is set up lower than the absolute value of the threshold of p channel MOS FET5, the absolute value of the threshold electrical potential difference of n channel MOS FET 3 and 4 is set up lower than the absolute value of the threshold of n channel MOS FET6 (a "threshold electrical potential difference" shall say the absolute value hereafter). And these MOSFETs 1-4 constitute the combinational circuit 11 of 2 input NAND gate. Moreover, it connects between supply voltage 12 and the imagination power-source line 9, and a control signal CSB 1 inputs p channel MOS FET5 into the gate, it connects between imagination earth wires 10 and grounds 13, and a control signal CS 1 inputs n channel MOS FET6 into the gate.

[0005] Next, actuation is explained. In operating the combinational circuit 11 of this 2 input NAND gate, while making a control signal CS 1 high-level, the control signal CSB 1 which is that reversal signal is made into a low level. Therefore, p channel MOS FET5 and n channel MOS FET6 will all be in the condition of ON, and can pull up the imagination power-source line 9 to the electrical-potential-difference VDD level of supply voltage 12, and, on the other hand, the imagination earth wire 10 is VGND of a ground 13. It is reduced to level. Consequently, this combinational circuit 11 will carry out the usual NAND actuation. Under the present circumstances, since the threshold electrical potential difference (absolute value) is set up low, also in case the electrical potential difference VDD of supply voltage 12 is a low battery, the high-speed actuation of MOSFETs 1-4 is attained.

[0006] When a combinational circuit 11 does not operate, a control signal CS 1 is made into a low level, and the control signal CSB 1 which is the reversal signal is made high-level. At this time, p channel MOS FET5 and n channel MOS FET6 all become off, and the imagination power-source line 9 and the imagination earth wire 10 are separated from supply voltage 12 and a ground 13, respectively. Since a threshold electrical potential difference (absolute value) is higher than MOSFETs 1-4 and p channel MOS FET5 and n channel MOS FET6 are set up by each at this time, leakage current can be suppressed small.

[0007] Generally, the electrical potential difference between the gate sources of MOSFET increases the leakage current between source drains exponentially to gate voltage in the field below a threshold electrical potential difference. For this reason, when the combinational circuit 11 is not operating, leakage current can be substantially reduced by giving a difference to the threshold electrical potential difference of MOSFETs 1–4 and MOSFETs 5 and 6. In addition, although drawing 7 shows as an example the case where a combinational circuit 11 is 2 input NAND gate, the argument with this same in the circuit of any classes which constitute LSI, and magnitude is materialized.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, since according to invention according to claim 1 the 1st field-effect transistor currently used for the sequential circuit was constituted so that a control means could make the threshold electrical potential difference adjustable A low power can perform writing and read-out of the data to the storage maintenance node which made low the threshold electrical potential difference of the 1st field-effect transistor, and was formed in this sequential circuit when a sequential circuit operated at a high speed. In addition, when a sequential circuit does not operate, by raising the threshold electrical potential difference of the 1st field-effect transistor, leakage current can be decreased and there is effectiveness which does not break and disappear the data currently held by this at the storage maintenance node. Moreover, since the switching means was constituted so that it could separate from other circuit parts when a combinational circuit did not operate, it is effective in the ability to reduce the leakage current of a combinational circuit.
[0045] Since according to invention according to claim 2 the 1st field-effect transistor which constitutes a sequential circuit was constituted so that it might have a backgate, when not operating a sequential circuit, and a control means controls the potential through a backgate, the threshold of the 1st field-effect transistor can be raised, leakage current can be decreased, and it is effective in bringing about prevention and low-power-izing of destruction and disappearance in the data currently held by this at the storage maintenance node.
[0046] Since according to invention according to claim 3 it constituted so that the control means linked to a sequential circuit might contain a forward voltage generator and a negative voltage generator, the control signal inputted into the forward voltage generator and the negative voltage generator linked to a backgate can make adjustable the threshold of the 1st field-effect transistor of the p channel section which constitutes a sequential circuit from high level or a low level, and the n channel section. therefore, since a transistor is operated with a low threshold when operating a sequential circuit, when there is little the power consumption, it moreover ends with rapid access and it does not operate on the other hand While making it become higher than supply voltage, the threshold of the transistor of the p channel section Since the threshold of the transistor of the n channel section can be made lower than ground potential, the leakage current which flows from the power source of a sequential circuit to a ground can be reduced, and there is effectiveness which does not disappear the maintenance data which are in a storage maintenance node by this. Furthermore, if a sequential circuit is constituted using the transistor which has the above-mentioned backgate, since a threshold is able to constitute this from a small transistor, reduction of a manufacturing cost is brought about by reduction of the routing counter accompanying reduction of the number of masks, and since the chip size of the semiconductor integrated circuit equipment of completion can moreover be decreased, it is effective in improving the product yield.
[0047] According to invention according to claim 4, since it is constituted so that smaller than the threshold electrical potential difference of the 3rd field-effect transistor used for the switching means, the threshold electrical potential difference of the 2nd field-effect transistor used for the combinational circuit is effective in the ability of a low power to perform logic actuation at a high speed only by stopping the level of the control signal sent to the gate of a combinational circuit.
[0048] According to invention according to claim 5, the threshold electrical potential difference of

the 2nd field-effect transistor used for the combinational circuit Spread a threshold electrical potential difference of the 3rd field-effect transistor, abbreviation, etc. which are used for the switching means. Since the 3rd field-effect transistor was constituted so that the electrical potential difference between the gate sources might be made into a reverse bias with the transistor by the side of supply voltage, and the transistor by the side of a ground when it was in an OFF state A transistor with a small threshold is applicable just like that by which the transistor used for the above-mentioned switching means is also used for a combinational circuit. Therefore, since the transistor which has the threshold of varieties in one semiconductor integrated circuit is not made intermingled, the number of masks is decreased, a fabrication process is simplified, and it is effective in reducing a manufacturing cost.

[0049] According to invention according to claim 6, a combinational circuit consists of two or more circuit blocks. The switching means is connected according to the individual to each circuit block. Since it constituted as the control means which makes adjustable the threshold electrical potential difference of the 1st field-effect transistor by which a sequential circuit also consists of two or more circuit blocks, and is included in each circuit block was connected according to the individual There is effectiveness which can control leakage current finely and can be prevented from disappearing the storage maintenance data of a sequential circuit taking into consideration terms and conditions, such as power consumption, an access rate, etc. of a semiconductor integrated circuit.

[0050] Since according to invention according to claim 7 the 1st booster and pressure-lowering machine can control independently the potential built between the gate sources of the 3rd field-effect transistor which a switching means has by the power-source and ground side, respectively in case a control signal goes via a reversal means and a noninverting means, it can consider as a reverse bias mutually. Since the leakage current of a combinational circuit can be reduced by addition of a simple circuit by this, there is effectiveness which contributes to low-power-ization.

[0051] According to invention according to claim 8, the control means linked to a sequential circuit is equipped with the 2nd pressure-lowering machine connected with the 2nd booster connected with a forward voltage generator, and a negative voltage generator. Since the forward voltage generator and the negative voltage generator were constituted so that it might consist of a simple multiplexer circuit, when a sequential circuit does not operate, the control signal which went via the multiplexer circuit can be set up so that the leakage current of a sequential circuit may be reduced more by the booster and pressure-lowering machine side through a backgate. Therefore, it is effective in the ability to reduce the power consumption of a circuit further only by adding a simple and cheap circuit, without disappearing storage maintenance data.

[0052] Since it was made for the booster and pressure-lowering machine contained in a control means to constitute independently of what is contained in a switching means according to invention according to claim 9, output voltage can be set up according to an individual, reduction of finer leakage current can be realized, and there is effectiveness which contributes to power-saving of the done whole semiconductor integrated circuit equipment.

[0053] Since according to invention according to claim 10 it constituted as the logical circuit including the circuit containing a booster and a pressure-lowering machine, and a combinational circuit and a sequential circuit joined together, if the booster and pressure-lowering machine of an integrated circuit are diverted to this logical circuit, since setting out of an additional circuit is omissible,-izing of the chip size of the whole semiconductor integrated circuit equipment can be carried out [****]. And there is effectiveness which can contribute also to reduction of the fabrication cost per one-sheet wafer by reduction in a chip size.

[0054] Since according to invention according to claim 11 it constituted so that the integrated circuit which has a booster and a pressure-lowering machine might consist of dynamic random access memory (DRAM), the hybrid circuit of a logical circuit and DRAM can be created, and since DRAM possesses a booster and a pressure-lowering machine for refresh actuation etc., it can usually be designed so that these may be used for logical circuit actuation. Therefore, there is effectiveness which cannot cause buildup of the number of components and can contribute to cutback-ization of the occupancy area of the whole hybrid circuit.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since the semiconductor integrated circuit of the conventional low-battery actuation mold was constituted as mentioned above, in the case of the combinational circuit where it opts for an output with the combination of an input, it operated normally like 2 input NAND gate, but in the case of the sequential circuit which has the function which carries out storage maintenance of the former condition, the technical problem of causing malfunction occurred.
[0009] Drawing of the so-called latch circuit which the input and output of two inverters crossed mutually and was connected to drawing 8 as an example of this sequential circuit is shown. In drawing, p channel MOS FET, and 16 and 17 are n channel MOS FET, and 14 and 15 have a low threshold electrical potential difference (absolute value) for all. 5 is p channel MOS FET, 6 is n channel MOS FET, and both sides consist of what has a high threshold electrical potential difference (absolute value). A sequential circuit 20 is constituted by these MOSFETs 14-17, nodes 18 and 19 form the storage maintenance node of a couple, and when one of these is high-level, the value which another side was set to a low level and inputted can be held.
[0010] Next, actuation is explained. When a sequential circuit 20 operates where CSB1 is set to a low level while CS1 is high-level, the value of the written-in data is held normally, and since both the threshold electrical potential differences of p channel MOS FET 14 and 15 and n channel MOS FET 16 and 17 are low, moreover, writing and read-out to nodes 18 and 19 can be performed at a high speed.
[0011] If CS1 is moreover set to CSB1 being high-level with a low level and leakage current decreases, while not operating, since the direction of the leakage current at the time of the OFF in MOSFETs 14-17 will become larger than the leakage current at the time of OFF of MOSFETs 5 and 6, it becomes impossible however, to hold the data of nodes 18 and 19. It is because the node 18 high-level [a node 18 is high-level, and] by the favor of leakage current which flows p channel MOS FET15 and n channel MOS FET16 although p channel MOS FET15 and n channel MOS FET16 will become off among MOSFETs 14-17 and other two will become ON, supposing a node 19 is a low level falls, for example and the node 19 of a low level goes up. This will continue until the level of nodes 18 and 19 becomes equal, and the data currently held as a result will be lost. Thus, in the semiconductor integrated circuit of the conventional low-battery actuation mold, the technical problem that the data of a sequential circuit will disappear occurred.
[0012] It aims at obtaining the semiconductor integrated circuit which can attain low-power-ization by reduction of the leakage current of the circuit which is not operating, without having been made in order that this invention might solve the above technical problems, and destroying the maintenance data of a sequential circuit.

[Translation done.]

MEANS

[Means for Solving the Problem] The semiconductor integrated circuit concerning invention according to claim 1 is equipped with a switching means, the combinational circuit connected to this switching means, the sequential circuit containing the 1st field-effect transistor, and the control means which makes adjustable the threshold electrical potential difference of the 1st field-effect transistor.
[0014] The 1st field-effect transistor in which the semiconductor integrated circuit concerning invention according to claim 2 is contained in a sequential circuit has the backgate, and a control means makes adjustable the threshold electrical potential difference of said 1st field-effect transistor through this backgate.
[0015] In the semiconductor integrated circuit concerning invention according to claim 3, a control means contains a forward voltage generator and a negative voltage generator.
[0016] The 3rd field-effect transistor is contained in the switching means, and the semiconductor integrated circuit concerning invention according to claim 4 has the absolute value of the threshold electrical potential difference of the 3rd field-effect transistor higher than the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor while the 2nd field-effect transistor is contained in the combinational circuit.
[0017] The semiconductor integrated circuit concerning invention according to claim 5 The 2nd field-effect transistor is contained in the combinational circuit, and 3rd at least two field-effect transistor is contained in the switching means. In the semiconductor integrated circuit by which the source of the transistor of another side is connected to ground potential while the source of the transistor of one of these is connected to supply voltage The absolute value of the threshold electrical potential difference of the 3rd field-effect transistor spreads [the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor] abbreviation etc. And when the 3rd field-effect transistor of the above is in an OFF state, let potential between the gate sources be a reverse bias with the transistor by the side of supply voltage, and the transistor by the side of a ground.
[0018] It consists of the 1st circuit block of plurality [semiconductor integrated circuit / concerning invention according to claim 6 / combinational circuit], and the control means to which a switching means makes adjustable the threshold electrical potential difference of the 1st field-effect transistor which it connects according to the individual, and a sequential circuit also consists of two or more 2nd circuit blocks, and is contained in each 2nd circuit block is connected according to the individual to each 1st circuit block.
[0019] The semiconductor integrated circuit concerning invention according to claim 7 is equipped with the reversal means connected with the 1st booster made to generate an electrical potential difference higher than supply voltage, the 1st pressure-lowering machine which generates an electrical potential difference lower than ground potential, and the 1st booster, and the noninverting means connected with the 1st pressure-lowering machine by the switching means.
[0020] As for the semiconductor integrated circuit concerning invention according to claim 8, the control means is equipped with the 2nd booster connected with a forward voltage generator, and the 2nd pressure-lowering machine connected with a negative voltage generator, and a forward voltage generator and a negative voltage generator consist of a multiplexer circuit.

[0021] The semiconductor integrated circuit concerning invention according to claim 9 differs from the 1st booster and the 1st pressure-lowering machine with which the 2nd booster and the 2nd pressure-lowering machine which are contained in a control means are contained in a switching means.
[0022] In the semiconductor integrated circuit equipped with the integrated circuit which has a logical circuit including a combinational circuit and a sequential circuit, and a booster and a pressure-lowering machine, the semiconductor integrated circuit concerning invention according to claim 10 drives the control means controlled through the backgate of a field-effect transistor which has the backgate contained in a sequential circuit while driving the switching means of a combinational circuit using the booster and pressure-lowering machine of an integrated circuit.
[0023] The integrated circuit with which the semiconductor integrated circuit concerning invention according to claim 11 has a booster and a pressure-lowering machine consists of dynamic random access memory (DRAM).
[0024]
[Embodiment of the Invention] Hereafter, one gestalt of implementation of this invention is explained.
Gestalt 1. drawing 1 of operation is drawing showing the semiconductor integrated circuit of the low-battery actuation mold by the gestalt 1 of implementation of this invention, and, for p channel MOS FET and 5, p channel MOS FET, and 3 and 4 is [1 and 2 / n channel MOS FET 23 and 24 of n channel MOS FET and 6] the nodes for backgates in drawing. Here, while the absolute value of the threshold electrical potential difference of p channel MOS FET 1 and 2 is set up lower than the absolute value of the threshold electrical potential difference of p channel MOS FET5, the absolute value of the threshold electrical potential difference of n channel MOS FET 3 and 4 is set up lower than the absolute value of the threshold electrical potential difference of n channel MOS FET6 (a "threshold electrical potential difference" shall say the absolute value hereafter). And these MOSFETs 1-4 constitute a combinational circuit 11 like 2 input NAND gate, and MOSFETs 5 and 6 constitute a switching means. In this case, it connects between supply voltage 12 and the imagination power-source line 9, and a control signal CSB 1 inputs p channel MOS FET5 into that gate. Moreover, it connects between imagination earth wires 10 and grounds 13, and a control signal CS 1 inputs n channel MOS FET6 into the gate.
[0025] On the other hand, as for 14 and 15, p channel MOS FET, and 16 and 17 are n channel MOS FET, and these constitute the sequential circuit 20. Moreover, the forward voltage generator 21, the negative voltage generator 22, and the nodes 23 and 24 for backgates of MOSFETs 14-17 constitute the control means. These MOSFETs 14-17 consist of what has the low absolute value of a threshold electrical potential difference, and nodes 18 and 19 form the storage maintenance node of a couple. In this case, it has the composition of having connected the backgate potential VC 1 of p channel MOS FET 14 and 15 to the output of the forward voltage generator 21, and having connected the backgate potential VD1 of n channel MOS FET 16 and 17 to the output of the negative voltage generator 22.
[0026] Next, actuation is explained. In operating a combinational circuit 11, while making a control signal CS 1 high-level, the control signal CSB 1 which is the reversal signal is made into a low level. Thereby, p channel MOS FET5 and n channel MOS FET6 will all be in the condition of ON, and can pull up the imagination power-source line 9 to the potential VDD level of supply voltage 12, and, on the other hand, the imagination earth wire 10 is VGND of a ground 13. It is reduced to level. Consequently, the combinational circuit 11 of such a 2 input NAND gate will carry out the usual NAND actuation. Under the present circumstances, since the threshold electrical potential difference (absolute value) of MOSFETs 1-4 is set up low, also in case the electrical potential difference of supply voltage 12 is a low battery, the high-speed actuation of it is attained with a low power.
[0027] In not operating a combinational circuit 11, a control signal CS 1 is made into a low level, and it makes high-level the control signal CSB 1 which is the reversal signal. At this time, p channel MOS FET5 and n channel MOS FET6 all become off, and the imagination power-source line 9 and the imagination earth wire 10 are separated from supply voltage 12 and a ground 13, respectively. Here, since p channel MOS FET5 and n channel MOS FET6 are set up more highly

than MOSFETs 1–4 by each in the threshold electrical potential difference (absolute value), they can suppress leakage current small.
[0028] On the other hand, while the control signal CS 2 inputted into a control means becomes high–level at the time of actuation and the backgate potential VC 1 of p channel MOS FET 14 and 15 serves as supply voltage VDD level with the forward voltage generator 21 about a sequential circuit 20, the backgate potential VD1 of n channel MOS FET 16 and 17 is the ground potential VGND by the negative voltage generator 22. It is set to level. Therefore, a sequential circuit 20 can perform the usual storage maintenance actuation at this time. In this case, since p channel MOS FET 14 and 15 and n channel MOS FET 16 and 17 of a sequential circuit 20 have the all low absolute value of a threshold electrical potential difference and are constituted, they can perform writing and read–out of the data to nodes 18 and 19 at a high speed. Moreover, when a sequential circuit 20 does not operate, CS2 is set to a low level, the output VC 1 of the forward voltage generator 21 becomes higher than supply voltage VDD, and the output VD1 of the negative voltage generator 22 is the ground potential VGND. It becomes a low value. Consequently, since the threshold electrical potential difference becomes high since the backgate potential VC 1 of p channel MOS FET 14 and 15 becomes higher than supply voltage 12, and the backgate potential VD1 concerning the backgate of n channel MOS FET 16 and 17 becomes [potential] lower than supply voltage 12, a threshold electrical potential difference becomes high too. For this reason, the leakage current which flows from the supply voltage 12 of a sequential circuit 20 to a ground 13 can be reduced.
[0029] As mentioned above, according to the gestalt 1 of this operation, it is effective in decreasing power consumption, without reducing leakage current and destroying the data of a storage maintenance node by changing the backgate potential of low threshold MOSFET and raising that threshold electrical potential difference, when not operating a sequential circuit 20. Furthermore, since the threshold of MOSFET currently used for the combinational circuit 11 and the sequential circuit 20 is low, there is effectiveness that a high speed and a low power can perform writing and read–out, also at the time of actuation. In addition, although the gestalt 1 of this operation explained control signals CS1 and CS2 as another signal, even if both are the same signals, same actuation can be realized, and the same effectiveness is done so.
[0030] Gestalt 2. drawing 2 of operation is drawing showing the semiconductor integrated circuit of the low–battery actuation mold by the gestalt 2 of implementation of this invention, and in drawing, since the configuration and actuation of a sequential circuit 20 are the same as that of the gestalt 1 of operation, they give the same sign to the same part, and omit duplication explanation. In the gestalt 2 of this operation, the threshold electrical potential difference of MOSFETs 5 and 6 for leakage current reduction in case a combinational circuit 11 does not operate is set as the same low threshold electrical potential difference as other MOSFETs 1–4.
[0031] Next, actuation is explained. When not operating a combinational circuit 11 with the gestalt 2 of this operation, it is Ground VGND about a control signal CS 1. While considering as low potential, reduction of leakage current is aimed at by making CSB1 into potential higher than supply voltage VDD. Otherwise, it is because the threshold of MOSFET which constitutes a switching means is comparable as what constitutes a combinational circuit, so leak of a current occurs between a power source and a ground and the consumed electric power of the whole circuit increases the way things stand. Therefore, if constituted as mentioned above, the same effectiveness as the gestalt 1 of operation is not only acquired, but a threshold can make all low including MOSFETs 5 and 6 used for a switching means, without using MOSFET which has two or more kinds of threshold electrical potential differences. Therefore, the number of masks can be decreased at the time of a fabrication of semiconductor integrated circuit equipment, and since a fabrication routing counter can be reduced, there is effectiveness of manufacturing–cost reduction.

[0032] Gestalt 3. drawing 3 of operation is the block diagram showing the case where the circuit block which consists of the combinational circuit and sequential circuit of each plurality by the gestalt 3 of implementation of this invention is applied to a large–scale integrated circuit (LSI), and is set to drawing. 111–11m It is the block of a combinational circuit and each is a control signal CSB 11 – CSB1m. 51–5m of p channel MOS FET to input A control signal CS 11 – CS1m 61–6m of

n channel MOS FET to input It provides. On the other hand, it is 201–20n. It is the block of a sequential circuit and each is CS21 – CS2n. 211–21n of forward voltage generators to input, 221–22n of negative voltage generators Node for backgates

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[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is circuitry drawing of the semiconductor integrated circuit by the gestalt 1 of implementation of this invention.
[Drawing 2] It is circuitry drawing of the semiconductor integrated circuit by the gestalt 2 of implementation of this invention.
[Drawing 3] It is circuitry drawing of the semiconductor integrated circuit by the gestalt 3 of implementation of this invention.
[Drawing 4] It is circuitry drawing of the semiconductor integrated circuit by the gestalt 4 of implementation of this invention.
[Drawing 5] It is circuitry drawing of the semiconductor integrated circuit by the gestalt 5 of implementation of this invention.
[Drawing 6] It is circuitry drawing of the semiconductor integrated circuit by the gestalt 6 of implementation of this invention.
[Drawing 7] It is circuitry drawing of the low-battery actuation circuit by conventional MT-CMOS.
[Drawing 8] It is circuitry drawing of the conventional latch circuit.
[Description of Notations]
5 P Channel MOS FET (Switching Means), 6 N Channel MOS FET (Switching Means), 11 A combinational circuit, 12 14 Supply voltage, 15 P channel MOS FET (control means), 16 17 N channel MOS FET (control means), 20 Sequential circuit, 21,211-21n A forward voltage generator (control means), 22,221-22n A negative voltage generator (control means), 23, 24,231-23n, 241-24n The node for backgates (control means), 48 A booster (the 1st booster, the 2nd booster), 49 A pressure-lowering machine (the 1st pressure-lowering machine, 2nd pressure-lowering machine), 581-58n, 591-59n Multiplexer circuit.

[Translation done.]

* NOTICES *

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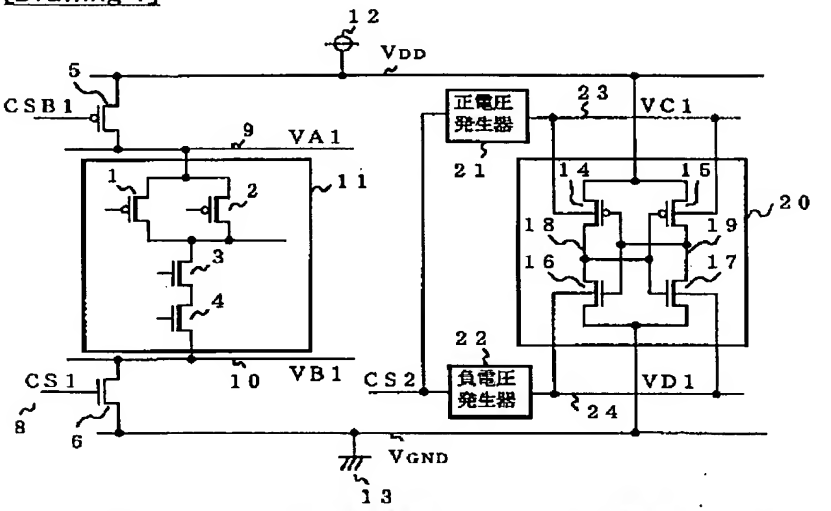
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

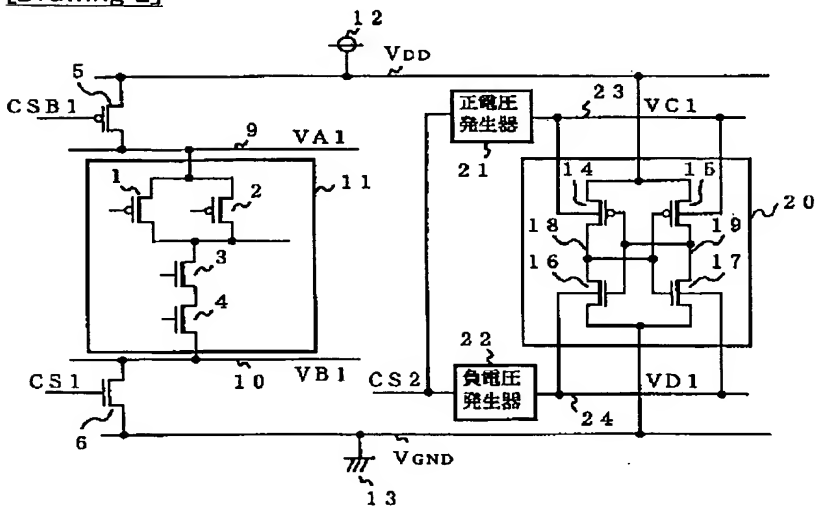
DRAWINGS

[Drawing 1]

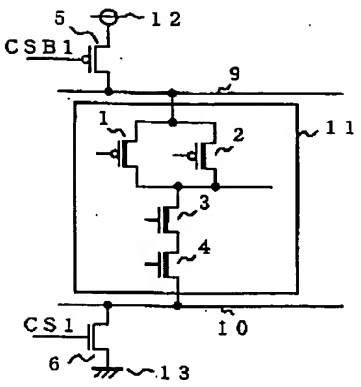


5：pチャネルMOSFET（スイッチング手段）
6：nチャネルMOSFET（スイッチング手段）
11：組み合わせ回路
12：電源電圧
14，15：pチャネルMOSFET（制御手段）
16，17：nチャネルMOSFET（制御手段）
20：順序回路
21：正電圧発生器（制御手段）
22：負電圧発生器（制御手段）
23，24：バックゲート用ノード（制御手段）

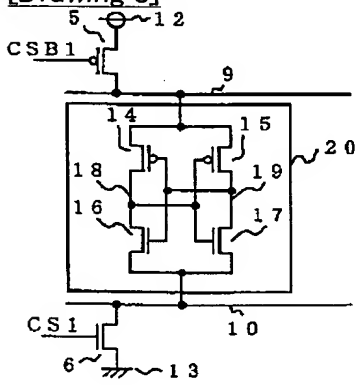
[Drawing 2]



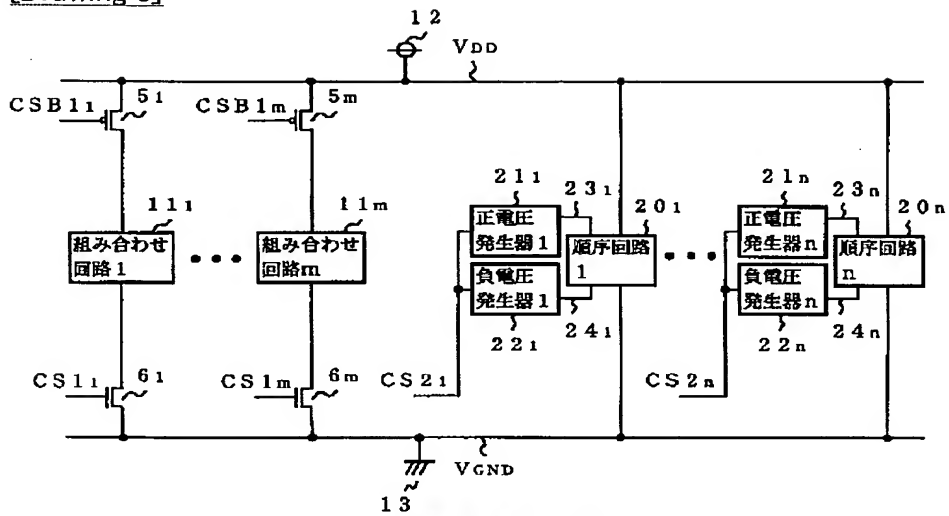
[Drawing 7]



[Drawing 8]

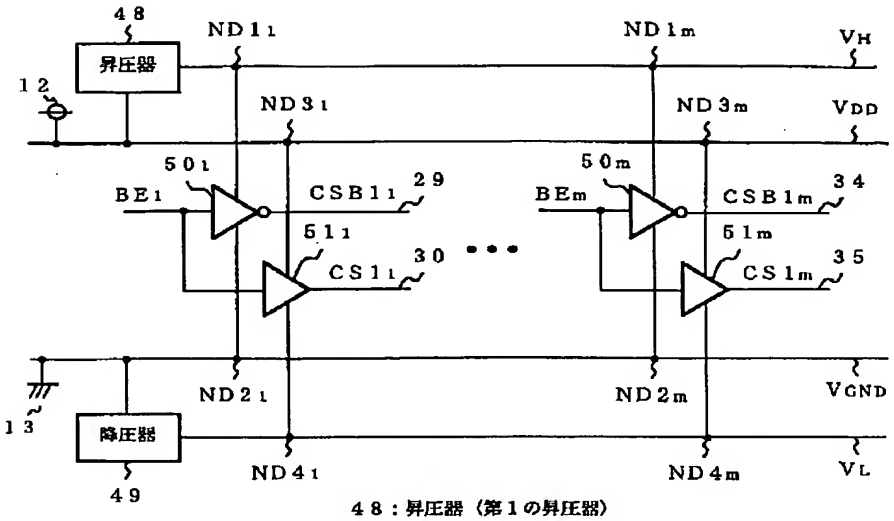


[Drawing 3]



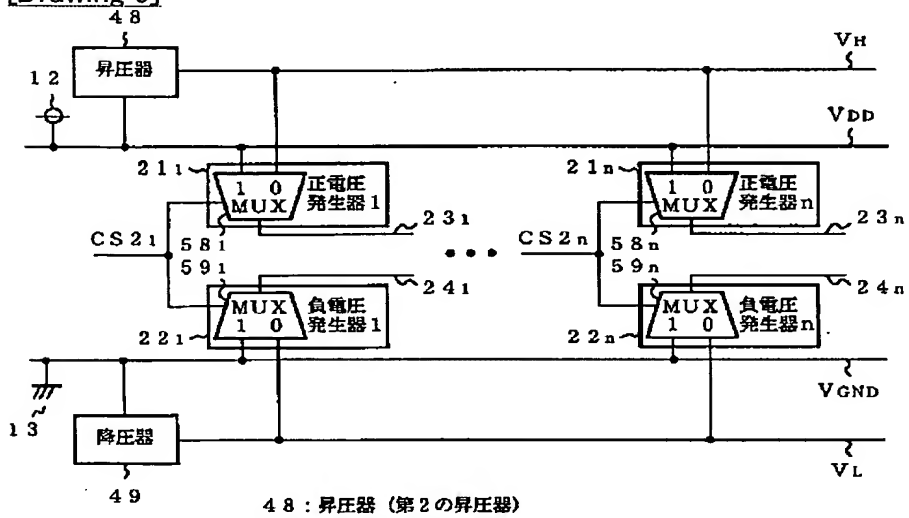
211～21n：正電圧発生器（制御手段）
221～22n：負電圧発生器（制御手段）
231～23n，241～24n：バックゲート用ノード（制御手段）

[Drawing 4]



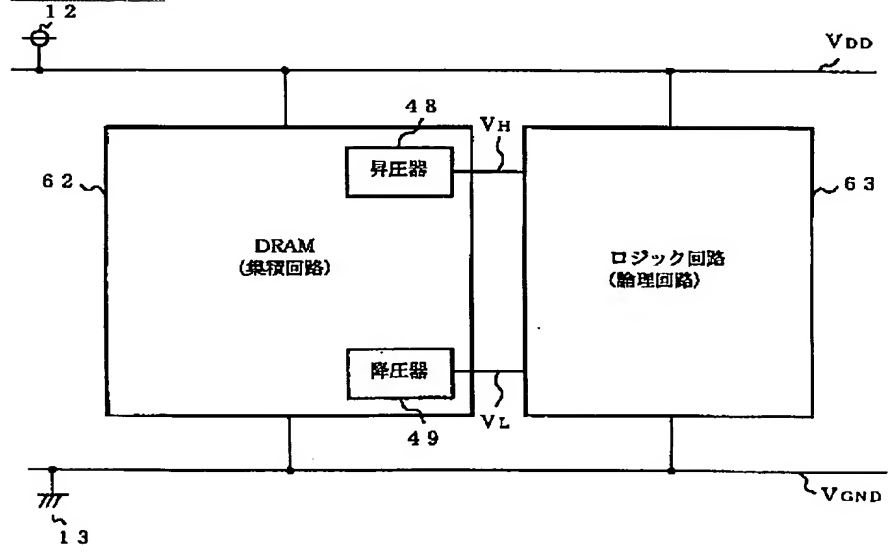
48：昇圧器（第１の昇圧器）
49：降圧器（第１の降圧器）

[Drawing 5]



48：昇圧器（第２の昇圧器）
49：降圧器（第２の降圧器）
581～58n.591～59n：マルチプレクサ回路

[Drawing 6]



[Translation done.]

CORRECTION OR AMENDMENT

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H01L 27/08 321 L
H03K 19/094 B

[Procedure amendment]
[Filing Date] November 7, Heisei 15 (2003. 11.7)
[Procedure amendment 1]
[Document to be Amended] Description
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[The content of amendment]
[Claim(s)]
[Claim 1]
The semiconductor integrated circuit equipped with the switching means, the combinational circuit connected to this switching means, the sequential circuit containing the 1st field-effect transistor, and the control means which makes adjustable the threshold electrical potential difference of the 1st field-effect transistor of the above.
[Claim 2]
It is the semiconductor integrated circuit according to claim 1 which the 1st field-effect transistor contained in a sequential circuit has the backgate, and is characterized by a control means making adjustable the threshold electrical potential difference of the 1st field-effect transistor of the above through this backgate.
[Claim 3]
A control means is a semiconductor integrated circuit according to claim 2 characterized by including a forward voltage generator and a negative voltage generator.

[Claim 4]
A semiconductor integrated circuit given [of claim 1 to the claims 3 which the 3rd field-effect transistor is contained in the switching means, and are characterized by the absolute value of the threshold electrical potential difference of the 3rd field-effect transistor of the above being higher than the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor of the above while the 2nd field-effect transistor is contained in the combinational circuit] in any 1 term.
[Claim 5]
The 2nd field-effect transistor is contained in the combinational circuit, and 3rd at least two field-effect transistor is contained in the switching means. In the semiconductor integrated circuit by which the source of the transistor of another side is connected to ground potential while the source of the transistor of one of these is connected to supply voltage The absolute value of the threshold electrical potential difference of the 3rd field-effect transistor of the above spreads [the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor of the above] abbreviation etc. And a semiconductor integrated circuit given [of claim 1 to the claims 3 characterized by making potential between the gate sources into a reverse bias with the transistor by the side of supply voltage, and the transistor by the side of a ground when the 3rd field-effect transistor of the above is in an OFF state] in any 1 term.
[Claim 6]
A combinational circuit is a semiconductor integrated circuit according to claim 1 characterized by consisting of two or more 1st circuit blocks, connecting the switching means according to the individual to each 1st circuit block, and connecting the control means which makes adjustable the threshold electrical potential difference of the 1st field-effect transistor by which a sequential circuit also consists of two or more 2nd circuit blocks, and is included in each 2nd circuit block according to an individual.
[Claim 7]
A switching means is a semiconductor integrated circuit according to claim 6 characterized by having the reversal means connected with the 1st booster made to generate an electrical potential difference higher than supply voltage, the 1st pressure-lowering machine which generates an electrical potential difference lower than ground potential, and the 1st booster of the above, and the noninverting means connected with the pressure-lowering machine of the above 1st.
[Claim 8]
A control means is a semiconductor integrated circuit according to claim 3 characterized by having the 2nd booster connected with a forward voltage generator, and the 2nd pressure-lowering machine connected with a negative voltage generator, and the above-mentioned forward voltage generator and a negative voltage generator consisting of a multiplexer circuit.
[Claim 9]
The semiconductor integrated circuit according to claim 8 characterized by the 2nd booster and the 2nd pressure-lowering machine which are contained in a control means differing from the 1st booster and the 1st pressure-lowering machine which are contained in a switching means.
[Claim 10]
The semiconductor integrated circuit characterized by driving the control means controlled through the backgate of a field-effect transistor which has the backgate contained in a sequential circuit in the semiconductor integrated circuit equipped with the integrated circuit which has a logical circuit including a combinational circuit and a sequential circuit, and a booster and a pressure-lowering machine while driving the switching means of a combinational circuit using the booster and pressure-lowering machine of the above-mentioned integrated circuit.
[Claim 11]
The semiconductor integrated circuit according to claim 10 characterized by the integrated circuit which has the above-mentioned booster and a pressure-lowering machine consisting of dynamic random access memory (DRAM).
[Claim 12]
The 1st electrical-potential-difference supply line which supplies the 1st electrical potential difference.

The 2nd electrical-potential-difference supply line which supplies the 2nd electrical potential difference,
The combinational circuit which connects with said 2nd electrical-potential-difference supply line, and has 1st at least one field-effect transistor,
A sequential circuit equipped with the latch circuit which is connected between said 1st electrical-potential-difference supply line and said 2nd electrical-potential-difference supply line, and has the 2nd field-effect transistor,
The 3rd field-effect transistor which is connected between said combinational circuit and said 1st electrical-potential-difference supply line, and controls supply of said 1st electrical potential difference to said combinational circuit according to the 1st control signal,
It has the voltage generator which generates the 3rd electrical potential difference, and has the control means which supplies selectively said the 1st electrical potential difference and said 3rd electrical potential difference to the backgate of said 2nd field-effect transistor according to the 2nd control signal,
Said 3rd electrical potential difference is a semiconductor integrated circuit characterized by being set up so that the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor may be increased.
[Claim 13]
The electrical-potential-difference supply line which supplies the 1st electrical potential difference,

A combinational circuit equipped with two or more 1st circuit blocks,
A sequential circuit equipped with two or more 2nd circuit blocks which contain respectively the latch circuit which has the 1st field-effect transistor connected to said electrical-potential-difference supply line,
Two or more 2nd field-effect transistors which are respectively prepared between said electrical-potential-difference supply line and said 1st circuit block, and are a flow and un-flowing selectively corresponding to said two or more 1st circuit blocks,
It has the control means which supplies selectively the 2nd electrical potential difference and said 1st electrical potential difference to the backgate of said 1st field-effect transistor,
Said control means is an electrical-potential-difference generation machine which generates said 2nd electrical potential difference by which bias was carried out from said 1st electrical potential difference so that the absolute value of the threshold electrical potential difference of said 1st field-effect transistor might be increased when said 2nd electrical potential difference was supplied to the backgate of said 1st field-effect transistor.
Preparation **********.
[Procedure amendment 2]
[Document to be Amended] Description
[Item(s) to be Amended] 0023
[Method of Amendment] Modification
[The content of amendment]
[0023]
The integrated circuit with which the semiconductor integrated circuit concerning invention according to claim 11 has a booster and a pressure-lowering machine consists of dynamic random access memory (DRAM).
The semiconductor integrated circuit concerning invention according to claim 12 The 1st electrical-potential-difference supply line which supplies the 1st electrical potential difference, and the 2nd electrical-potential-difference supply line which supplies the 2nd electrical potential difference, The combinational circuit which connects with the 2nd electrical-potential-difference supply line, and has 1st at least one field-effect transistor, A sequential circuit equipped with the latch circuit which is connected between the 1st electrical-potential-difference supply line and the 2nd electrical-potential-difference supply line, and has the 2nd field-effect transistor, The 3rd field-effect transistor which is connected between a combinational circuit and the 1st electrical-potential-difference supply line, and controls supply of the 1st electrical potential difference to a combinational circuit according to the 1st control signal, It has the voltage generator which

generates the 3rd electrical potential difference. To the backgate of the 2nd field-effect transistor It has the control means which supplies selectively the 1st electrical potential difference and 3rd electrical potential difference according to the 2nd control signal, and the 3rd electrical potential difference is set up so that the absolute value of the threshold electrical potential difference of the 2nd field-effect transistor may be increased.

The semiconductor integrated circuit concerning invention according to claim 13 The electrical-potential-difference supply line which supplies the 1st electrical potential difference, and a combinational circuit equipped with two or more 1st circuit blocks, A sequential circuit equipped with two or more 2nd circuit blocks which contain respectively the latch circuit which has the 1st field-effect transistor connected to an electrical-potential-difference supply line, Two or more 2nd field-effect transistors which are respectively prepared between an electrical-potential-difference supply line and the 1st circuit block, and are a flow and un-flowing selectively corresponding to two or more 1st circuit blocks, It has the control means which supplies selectively the 2nd electrical potential difference and 1st electrical potential difference to the backgate of the 1st field-effect transistor. A control means When the 2nd electrical potential difference is supplied to the backgate of the 1st field-effect transistor, it has the electrical-potential-difference generation machine which generates the 2nd electrical potential difference by which bias was carried out from the 1st electrical potential difference so that the absolute value of the threshold electrical potential difference of the 1st field-effect transistor might be increased.

[Translation done.]